CLAIMS

What is claimed is:

1. A computer system, comprising:

a host bus;

an input/output (I/O) fault-tolerant interconnect system; and

a core logic chipset comprising a configurable bridge interface connectable between the host bus and the I/O fault-tolerant interconnect system, the I/O fault-tolerant interconnect system comprising:

an I/O bus selectively comprising one of a first type bus and a second type bus, the I/O bus comprising a first bus portion and a second bus portion; and

a device interface connectable to the I/O bus, wherein the first device interface is configured to detect errors in a transaction received by the device interface, wherein,

if a first error is detected on the first bus portion, then the transaction is performed over the second bus portion; and

if a second error is detected on the second bus portion, then the transaction is performed over the first bus portion.

2. The system as recited in claim 1, wherein if both the first and second errors are detected, then the transaction is terminated.

3. The system as recited in claim 1, wherein the first error and the second error comprise parity errors.

4. The system as recited in claim 1, wherein the first type bus comprises an accelerated graphics port bus, and the second type bus comprises a peripheral component interconnect bus.

5. The system as recited in claim 4, wherein the peripheral component interconnect bus comprises a PCI-X bus.

6. The system as recited in claim 1, comprising a second input/output (I/O) bus, wherein the core logic chipset comprises a second bridge interface connectable between the host bus and the second I/O bus.

7. The system as recited in claim 6, wherein the second I/O bus comprises a peripheral component interconnect bus.

8. The system as recited in claim 1, wherein the transaction comprises an address phase and a data phase, and wherein the device interface is configured to detect errors during the address phase, and wherein,

if the first error is detected on the first bus portion, then the data phase is completed over the second bus portion; and

if the second error is detected on the second bus portion, then the data phase is completed over the first bus portion.

9. The system as recited in claim 1, wherein the device interface comprises a target interface, and the fault-tolerant interconnect system comprises an initiator interface connectable to the I/O bus, wherein

the initiator interface requests the target interface for the transaction to be performed over the first and second bus portions; and

the target interface responds to the initiator interface, whereby,

an acknowledge first and second portions signal indicates the transaction may be performed over the first and second bus portions;

an acknowledge first portion signal indicates the transaction may be performed over the first bus portion; and

an acknowledge second portion signal indicates the transaction may be performed over the second bus portion.

10. The system as recited in claim 9, wherein the acknowledge first and second portions signal is sent to the initiator interface only after the target interface determines that the first and second errors are not detected.

11. The system as recited in claim 9, wherein the acknowledge first portion signal is sent to the initiator interface only after the target interface determines that the first error is not detected.

12. The system as recited in claim 9, wherein the acknowledge second portion signal is sent to the initiator interface only after the target interface determines that the second error is not detected.

13. The system as recited in claim 1, wherein the I/O bus comprises a 64-bit bus, and wherein the first bus portion is a first 32-bit bus and the second bus portion is a second 32-bit bus.

14. The system as recited in claim 1, wherein the configurable bridge interface is configured in response to receipt of a configuration signal.

15. The system as recited in claim 14, wherein the configuration signal is generated by a hardwired jumper circuit.

16. The system as recited in claim 1, wherein the core logic chipset comprises at least one integrated circuit.

17. The system as recited in claim 16, wherein the at least one integrated circuit comprises at least one application specific integrated circuit.

18. The system as recited in claim 16, wherein the at least one integrated circuit comprises at least one programmable logic array integrated circuit.

19. The system as recited in claim 1, wherein the host bus and the I/O bus are disposed on a substrate.

20. The system as recited in claim 19, wherein the substrate is a printed circuit board.

21. The system as recited in claim 19, wherein the I/O bus is a universal bus comprising a plurality of universal conductive paths disposed on the substrate, and wherein the first type bus and the second type bus share common signals on the plurality of universal conductive paths.

22. The system as recited in claim 1, wherein the configurable bridge interface is configured for either the first type bus or the second type by software control of the core logic chipset.

23. The system as recited in claim 1, wherein the configurable bridge interface is configured for either the first type bus or the second type bus when either a first type device or a second type device, respectively, is detected on the I/O bus.

24. The system as recited in claim 23, wherein the first type device comprises an accelerated graphics port device, and the second type device comprises a peripheral component interconnect device.

25. The system as recited in claim 23, wherein the configurable bridge interface is configured during power on self test of the computer system.

26. The system as recited in claim 23, wherein the configurable bridge interface is configured during configuration of the computer system.

27. A computer system, comprising:

a host processor connected to a host bus;

a memory connected to a memory bus;

a first input/output (I/O) bus;

an input/output (I/O) fault-tolerant interconnect system; and

a core logic chipset comprising:

a first bridge interface between the host bus and the first I/O bus

a configurable second bridge interface between the host bus and the I/O fault-tolerant interconnect system, the I/O fault-tolerant interconnect system comprising:

a second input/output (I/O) bus comprising one of a first type bus and a second type bus, the second I/O bus comprising a first bus portion and a second bus portion; and

a device interface connected to the second I/O bus, wherein the device interface is configured to detect errors in a transaction received by the device interface, wherein,

if a first error is detected on the first bus portion, then the transaction is performed over the second bus portion; and

if a second error is detected on the second bus portion, then the transaction is performed the first bus portion.

28. The system as recited in claim 27, wherein if the first and second errors are detected, then the transaction is terminated.

29. The system as recited in claim 27, wherein the first and second errors comprise parity errors.

30. The system as recited in claim 27, wherein the first type bus comprises an accelerated graphics port bus, and the second type bus comprises a peripheral component interconnect bus.

31. The system as recited in claim 27, wherein the device interface comprises a target interface, and the fault-tolerant interconnect system comprises:

an initiator device interface connected to the second I/O bus, wherein the initiator interface requests the target interface for the transaction to be performed over the first and second bus portions; and

the target interface responds to the initiator interface, whereby,

an acknowledge first and second portions signal indicates the transaction may be performed over the first and second bus portions;

an acknowledge first portion signal indicates the transaction may be performed over the first bus portion; and

an acknowledge second portion signal indicates the transaction may be performed over the second bus portion.

32. The system as recited in claim 31, comprising a first peripheral component interconnect device connected to the second I/O bus, the first peripheral component interconnect device comprising the target interface.

33. The system as recited in claim 32, comprising a second peripheral component interconnect device connected to the second I/O bus, the peripheral second component interconnect device comprising the initiator interface.

34. The system as recited in claim 33, wherein the first and second peripheral component interconnect devices comprise first and second PCI-X devices.

35. The system as recited in claim 27, wherein the configurable bridge interface is configured in response to a configuration signal generated by a hardwired jumper circuit.

36. The system as recited in claim 27, wherein the configurable bridge interface is configured by software control of the core logic chipset.

38. The system as recited in claim 27, wherein the configurable bridge interface is configured for the first type bus if a first type device is detected connected to the second I/O bus.

39. The system as recited in claim 27, wherein the second bridge interface is configured for the second type bus if a second type device is detected connected to the second I/O bus.

40. A method of configuring a core logic chipset for connecting between a host bus and a fault-tolerant input/output (I/O) bus, the fault-tolerant I/O bus comprising either a first type bus or a second type bus, the method comprising the acts of:

providing a core logic chipset connected to a host bus and to a fault-tolerant I/O bus, the fault-tolerant I/O bus comprising either a first type I/O bus or a second type I/O bus, the fault-tolerant I/O bus comprising a first bus portion and a second bus portion;

configuring the core logic chipset to interface between either the first type bus or the second type bus;

providing a device interface connected to the fault-tolerant I/O bus;

determining occurrence of an error in a transaction received by the device interface on the fault-tolerant I/O bus;

performing the transaction over the second bus portion if occurrence of a first error is determined on the first bus portion; and

performing the transaction over the first bus portion if occurrence of a second error is determined on the second bus portion.

41. The method as recited in claim 40, comprising terminating the transaction if occurrence of both the first and second errors is determined.

42. The method as recited in claim 40, wherein the first and second errors comprise parity errors.

43. The method as recited in claim 40, comprising the acts of:

providing a second device interface connected to the fault-tolerant I/O bus;

transmitting a request from the second device interface to the first device interface for the transaction to be performed over the first and second bus portions;

transmitting a response from the first device interface to the second device interface, the response comprising either:

an acknowledge first and second portions signal to indicate that the transaction may be performed over the first and second bus portions;

an acknowledge first portion signal to indicate that the transaction may be performed over the first bus portion; or

an acknowledge second portion signal to indicate that the transaction may be performed over the second bus portion.

44. The method as recited in claim 40, comprising the acts of:

configuring the core logic chipset to interface between the host bus and the first type bus if a first configuration signal is applied to the core logic chipset; and

configuring the core logic chipset to interface between the host bus and the second type bus if a second configuration signal is applied to the core logic chipset.

45. The method as recited in claim 44, wherein the first type bus comprises a peripheral component interconnect bus, and the second type bus comprises an accelerated graphics port bus.

46. The method as recited in claim 45, wherein the peripheral component interconnect bus comprises a PCI-X bus.

47. The method as recited in claim 45, comprising the act of generating the first configuration signal upon detection of a peripheral component interconnect device connected to the fault-tolerant I/O bus.

48. The method as recited in claim 45, comprising the act of generating the second configuration signal upon detection of an accelerated graphics port device connected to the fault-tolerant I/O bus.

49. The method as recited in claim 40, wherein the fault-tolerant I/O bus comprises a 64-bit bus, and the first bus portion comprises a first 32-bit bus and the second bus portion comprises a second 32-bit bus.

50. The method as recited in claim 40, wherein the first type bus comprises a peripheral component interconnect bus, and the second type bus comprises an accelerated graphics port bus.